FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC329.001AUS	APPLICATION NO. 10/817,310
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Catthoor et al.	
	FILING DATE April 2, 2004	GROUP 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
PD	1	B.Amrutur et al. "Speed and Power Scaling of SRAM's", IEEE Journal of Solid-state Circ., Vol. 35 No. 2, pp.175- 185, Feb. 2000.
PD	2	E.Brockmeyer et al. "Systematic Cycle budget versus System Power Trade-off: a New Perspective on System Exploration of Real-time Data-dominated Applications", Proc. IEEE Intnl. Symp. on Low Power Design, Rapallo, Italy, pp.137-142, Aug. 2000.
PD	3	J.A.Davis et al. "Interconnect limits on gigascale integration (GSI) in the 21st century", Proc. of the IEEE, No.3, Vol.89, pp:305-324, March 2001.
PD	4	R.Ho et al. "The future of wires", Proc. Of the IEEE, Vol.89, No.4, pp.490-504, April 2001.
PD	5	K.Itoh et al., "Limitations and challenges of multi-gigabit DRAM chip design", IEEE J. of Solid-state Circ., Vol. 32, No. 5, pp.624-634, May 1997.
PD	6	D.Sylvester et al., "Impact of small process geometries on microarchitectures in systems on a chip", Proc. of the IEEE, Vol.89, No.4, pp.467-489, April 2001.

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*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
PD	7	A. Vandecappelle et al., "Global Multimedia System Design Exploration using Accurate Memory Organization Feedback" Proc. 36th ACM/IEEE Design Automation Conf., New Orleans LA, pp.327-332, June 1999.
PD	8	S.J.E.Wilton et al., "CACTI: An enhanced cache access and cycle time model", IEEE J. of Solid State Circuits, Vol.31, No.5, pp.677-688, May 1996.
PD	9	S. Wuytack et al., "Minimizing the Required Memory Bandwidth in VLSI System Realizations", IEEE Trans. on VLSI Systems, Vol.7, No.4, pp.433-441, Dec. 1999.
PD	10	R. J. Evans et al., "*Energy Consumption Modeling and Optimization for SRAM's*, IEEE Journal of Solid-State Circuits, Vol.30, No.4, pp.571-579, May 1995.
PD	11	T. Seki et al., *A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier*, IEEE Journal of Solid-State Circuits, Vol.28, No.4, pp. 478-483, April 1993.
PD	12	A. P. Chandrakasan et al., "*Low-Power CMOS Digital Design*", IEEE Journal of Solid-State Circuits, no.4, vol.27, pp. 473, April 1992.
PD	13	J. Lachman et al., "A 500MHz 1.5MB cache with on-chip CPU", Proceedings of the ISSC Conference (1999) p. 192.
PD	14	A. Chandrakasan et al., "A Low Power Chipset for Portable Multimedia Applications", (1994) IEEE International Solid-State Circuits Conf., pgs 82-83.
PD	15	A. Papanikolaou et al., "Interconnect Exploration for Future Wire Dominated Technologies" (2002)
PD	16	http://research.compaq.com/wrl/people/jouppi/Cacti.h, "Cacti", Accessed prior to April 4, 2003 and retrieved after April 2, 2004.
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PD	19	Sylvester et al., "Getting to the Bottom of Deep Submicron II: A Global Wiring Paradigm". (1999)
PD	20	Doug Matzke, "Will Physical Scalability Sabotage Performance Gains?", (1997), pgs 37-39.
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PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	10/817,310
	Filing Date	April 2, 2004
	First Named Inventor	Cathoor et al.
	Art Unit	2825
(Multiple sheets used when necessary)	Examiner	~~Unassigned~~ Paul Dinh
SHEET 1 OF 1	Attorney Docket No.	IMEC329.001AUS

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[1]

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
PD	1	BROCKMEYER E ET AL: "Systematic cycle budget versus system power trade-off: a new perspective on system exploration of real-time data-dominated applications" LOW POWER ELECTRONICS AND DESIGN, 2000. ISLPED '00. PROCEEDINGS OF THE 2000 INTERNATIONAL SYMPOSIUM ON JULY 26-27, 2000, PISCATAWAY, NJ, USA,IEEE, 26 July 2000 (2000-07-26), pages 137-142, XP010517318 ISBN: 1-58113-190-9	
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PD	6	YUNSI FEI ET AL: "Functional partitioning for low power distributed systems of systems-on-a-chip" DESIGN AUTOMATION CONFERENCE, 2002. PROCEEDINGS OF ASP-DAC 2002. 7TH ASIA AND SOUTH PACIFIC AND THE 15TH INTERNATIONAL CONFERENCE ON VLSI DESIGN. PROCEEDINGS. BANGALORE, INDIA 7-11 JAN. 2002, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 7 January 2002 (2002-01-07), pages 274-281, XP010588114 ISBN: 0-7695-1441-3	

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Examiner Signature	/Paul Dinh/	Date Considered	06/03/2006

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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